The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ZHONG-NING (GEORGE) CAI

Appeal No. 2006-2707
Application No. 09/749,792

ON BRIEF

Before THOMAS, HAIRSTON, and HOMERE, ***Administrative Patent Judges***.

HOMERE, ***Administrative Patent Judge***.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 1 through 20, all of which are pending in this application.

We affirm.

Invention

Appellant's invention relates generally to a method and apparatus for performing dynamic power control of a processor (300) based on the thermal condition of the processor. First, a

thermal sensor (335) is used to measure the temperature of the processor (300), which is driven by a clock frequency (330). Next, a frequency reduction circuit (FRC) (305), upon determining that the processor temperature has reached a predetermined threshold, reduces the clock frequency of the processor to thereby allow the processor to cool off. The FRC (305) also includes a performance demanding level (PDL) module (311), which enables the FRC to determine the rate of reduction of the temperature-related frequency of the processor.

Claim 1 is representative of the claimed invention and is reproduced as follows:

1. An apparatus for dynamic power control of a processor based on a thermal condition, comprising:

a sensor to measure a thermal characteristic of a processor with a clock frequency;

a circuit to reduce the clock frequency of the processor responsive to the measured thermal characteristic satisfying a pre-determined threshold, the circuit including a performance demanding level input to determine a rate of the temperature-related frequency reduction.

References

The Examiner relies on the following references:

McDermott et al. (McDermott)	5,233,314	Aug. 3, 1993
Georgiou et al. (Georgiou)	5,940,785	Aug. 17, 1999

Ko	6,192,479	Feb. 20, 2001 (filed Jan. 19, 1995)

Rejections at Issue

A. Claims 1 through 4, 6 through 9 and 11 through 17 stand rejected under 35 U.S.C. § 103 as being unpatentable over the combination of Georgiou and McDermott.

B. Claims 5 and 10 stand rejected under 35 U.S.C. § 103 as being unpatentable over the combination of Georgiou, McDermott and Ko.

C. Claims 18 through 20 stand rejected under 35 U.S.C. § 103 as being unpatentable over the combination of Ko, Georgiou and McDermott.

Rather than reiterate the arguments of Appellant and the Examiner, the opinion refers to respective details in the Briefs[1] and the Examiner's Answers.[2] Only those arguments actually made by Appellant have been considered in this decision. Arguments that Appellant could have made but chose not to make in the

1 Appellant filed an Appeal Brief on October 24, 2005. Appellant filed a Reply Brief on April 3, 2006. Appellant filed a supplemental Reply Brief on July 27, 2006.
2 The Examiner mailed an Examiner's Answer on February 2, 2006. The Examiner mailed a supplemental Examiner's Answer on June 9, 2006.

Briefs have not been taken into consideration. See 37 CFR 41.37(c)(1)(vii)(eff. Sept. 13, 2004).

OPINION

In reaching our decision in this appeal, we have carefully considered the subject matter on appeal, the Examiner's rejections, the arguments in support of the rejections and the evidence of obviousness relied upon by the Examiner as support for the rejections. We have, likewise, reviewed and taken into consideration Appellant's arguments set forth in the Briefs along with the Examiner's rationale in support of the rejections and arguments in the rebuttal set forth in the Examiner's Answers. After full consideration of the record before us, we agree with the Examiner that claims 1 through 17 are properly rejected under 35 U.S.C. § 103 as being unpatentable over the combination of Georgiou and McDermott. Additionally, we agree with the Examiner that claims 18 through 20 are properly rejected under 35 U.S.C. § 103 as being unpatentable over the combination of Ko, Georgiou and McDermott. Accordingly, we affirm the Examiner's rejections of claims 1 through 20 for the reasons set forth **infra**.

I. Under 35 U.S.C. § 103(a), is the Rejection of Claims 1 through 4, 6 through 9 and 11 through 17 as being unpatentable over the combination of Georgiou and McDermott Proper?

In rejecting claims under 35 U.S.C. § 103, the Examiner bears the initial burden of establishing a **prima facie** case of obviousness. **In re Oetiker**, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). **See also In re Piasecki**, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984). The Examiner can satisfy this burden by showing that some objective teaching in the prior art or knowledge generally available to one of ordinary skill in the art suggests the claimed subject matter. **In re Fine**, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Only if this initial burden is met does the burden of coming forward with evidence or argument shift to the Appellants. **Oetiker**, 977 F.2d at 1445, 24 USPQ2d at 1444. **See also Piasecki**, 745 F.2d at 1472, 223 USPQ at 788. Thus, the examiner must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the examiner's conclusion. However, a suggestion, teaching, or motivation to combine the relevant prior art teachings does not have to be found explicitly in the prior art, as the teaching, motivation, or suggestion may

be implicit from the prior art as a whole, rather than expressly stated in the references. The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art. **In re Kahn**, 441 F.3d 977, 987-88, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006) citing **In re Kotzab**, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1316-17 (Fed. Cir. 2000). See also **In re Thrift**, 298 F.3d 1357, 1363, 63 USPQ2d 2002, 2008 (Fed. Cir. 2002).

An obviousness analysis commences with a review and consideration of all the pertinent evidence and arguments. "In reviewing the [E]xaminer's decision on appeal, the Board must necessarily weigh all of the evidence and argument." **Oetiker**, 977 F.2d at 1445, 24 USPQ2d at 1444. "[T]he Board must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the agency's conclusion." **In re Lee**, 277 F.3d 1338, 1344, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002).

With respect to representative claim 1, Appellant argues in the Briefs that neither Georgiou nor McDermott teaches a performance demanding level input for determining the rate of

reduction of the temperature-related frequency. Particularly, at page 8 of the Appeal Brief,[3] Appellant states the following:

> [A]t most the combination of Georgiou with McDermott yields Georgiou's device plus an improved PLL. The performance demanding level input to determine a rate of temperature-related frequency reduction, called for independent claims 1, 7 and 12, is totally absent from the combination of Georgiou and McDermott.

In order for us to decide the question of obviousness, "[t]he first inquiry must be into exactly what the claims define." **In re Wilder**, 429 F.2d 447, 450, 166 USPQ 545, 548 (CCPA 1970). "Analysis begins with a key legal question-- what is the invention claimed ?"...Claim interpretation...will normally control the remainder of the decisional process." **Panduit Corp. v. Dennison Mfg. Co.**, 810 F.2d 1561, 1567-68, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987).

We note that representative claim 1 reads in part as follows:

> [T]he circuit including a performance demanding level input to determine a rate of the temperature-related frequency reduction.

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3 We note that Appellant reiterates these same arguments at pages 2 through 4 of the Reply Brief and at pages 2 and 3 of the Supplemental Reply Brief.

We note at paragraph 20, Appellant's specification states the following:

> [0020] The performance demanding level signal (PDL) 311 is an input signal used by the frequency reduction circuit 305 to determine the level of sensitivity (or aggression) used for frequency reduction. If PDL signal 311 is asserted (e.g., value of "1"), then frequency reduction cannot be aggressive and instead fine granularity must be used (e.g., [fraction (1/15)] reduction from normal clock frequency) for reducing the normal clock frequency. Alternatively, if PDL signal 311 is not asserted (e.g., value of "0"), then frequency reduction can be aggressive and higher percentages of frequency reduction (e.g., close to 50% reduction from normal clock frequency) may be used for reducing the normal clock frequency. Advantageously, the PDL signal 311 can be used as a form of hardware performance profiling for system components interconnected to processor architecture 300.

Thus, the claim does require a performance demanding level input for determining the rate of reduction of the temperature-related frequency.

Now, the question before us is what Georgiou and McDermott would have taught to one of ordinary skill in the art? To answer this question, we find the following facts:

1. At column 4, lines 26 through 50, Georgiou states the following:

> The signal 125 from the thermal sensor is provided to a temperature decoder 130 which samples the signal and compares it to a predetermined temperature threshold to determine if the functional unit is overheating. The temperature decoder 130 generates a current/clock control signal 270 as a function of the comparison, e.g., **if the threshold has been exceeded or as a function of the temperature relative to a prior sample and/or rate of temperature change. The signal 270 is coupled to the adjustable on-chip voltage regulators 330 to reduce the supply voltage 325.** The signal 270 is also coupled to the clock selector 430 to cooperatively modulate the clock frequency sufficiently to maintain system synchronization at the reduced supply voltage. The output 325 of the adjustable voltage regulator 330 is applied to the voltage supply of the functional unit which provided the thermal signal 125. The modulated clock frequency 425 which corresponds to the reduced supply voltage 325 is applied to the clock inputs of the associated functional unit. The reduction in the voltage swing achieves the bulk of the reduction in the functional unit's power dissipation. **The clock frequency to the functional unit is correspondingly reduced to that which has been previously characterized to ensure system synchronization at the reduced voltage. The reduction in clock frequency advantageously provides further reductions in power dissipation. [Emphasis added].**

2. Further, at column 8, lines 55 through 66, Georgiou states the following:

> The clock selector includes a decoder 460 which receives signal 270 associated with a particular functional unit via its thermal sensor 119 and the temperature decoder 130. The decoder 460 decodes the signal 270 and outputs a clock select signal 465 to a select input (S) to the multiplexer associated with the particular functional unit. **The clock select signal 465 is used to select the clock frequency corresponding to the voltage output by voltage regulator 330 according to signal 270.** The clock selector also includes a multiplexor selector which selects and latches signal 465 into the appropriate multiplexor 470 according to functional unit address 280. (Emphasis Added)

With the above discussion in mind, we find that Georgiou teaches a method and apparatus for keeping a processor from overheating. Particularly, Georgiou teaches a thermal sensor and a comparator for determining when the temperature of the processor has exceeded a predetermined threshold (i.e overheating). Further, Georgiou discloses that upon receipt of a signal (270) from the comparator indicating that the processor is overheating, the voltage regulators (330) reduce the supply voltage, and the clock selector (430) selects a modulated clock frequency (425) that correspondingly reduces the clock frequency

down to a rate that can reduce the amount of power dissipated in the processor.

It is our view that one of ordinary skill in the art would have duly recognized that Georgiou's teaching of a clock selector that selects a reduced clock frequency in response to an indication that the processor is overheating amounts to the claimed limitation of a PDL input that determines the rate of reduction of a temperature-related frequency. The ordinarily skilled artisan would have readily been apprised of the fact that by selecting a reduced clock frequency to prevent further power dissipation in the processor, the frequency selector disclosed in Georgiou must necessarily select a reduced frequency rate that is capable of reducing the temperature of the processor.

As to McDermott, his teaching of determining the rate of change for advancing or retarding the output frequency is limited to improving the performance of a PLL circuit, notwithstanding the temperature of the processors used such inter-chip communications. We find, however, that the Examiner's reliance upon McDermott for the cited teaching was cumulative since Georgiou discloses such teaching. It is our view that since Georgiou teaches a performance demanding level input for determining the rate of reduction of the temperature-related

frequency, McDermott is cumulative to a proper rejection under 35 U.S.C. § 103 of representative claim 1, as Georgiou discloses all that is claimed. It is therefore our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would have suggested to the ordinarily skilled artisan the invention as set forth in representative claim 1. Accordingly, the Examiner's obviousness rejection of claims 1 through 4, 6 through 9 and 11 through 17 is sustained.

II. Under 35 U.S.C. § 103(a), is the Rejection of Claims 5 and 10 as being unpatentable over the combination of Georgiou, McDermott and Ko Proper?

With respect to claims 5 and 10, Appellant argues in the Appeal Brief that the combination of Georgiou and McDermott does not disclose a performance demanding level input for determining the rate of reduction of the temperature-related frequency. We have already addressed this argument in the discussion of claim 1 above, and we do not agree with Appellant. Further, Appellant argues that Ko does not cure the deficiencies of the Georgiou-McDermott combination. As noted above, we find no such deficiencies in the Georgiou reference for Ko to remedy. It is therefore our view, after consideration of the record before us,

that the evidence relied upon and the level of skill in the particular art would have suggested to the ordinarily skilled artisan the invention as set forth in claims 5 and 10. Accordingly, the Examiner's obviousness rejection of claims 5 and 10 is sustained.

III. Under 35 U.S.C. § 103(a), is the Rejection of Claims 18 through 20 as being unpatentable over the combination of Ko, Georgiou, McDermott Proper?

With respect to claims 18 through 20, Appellant argues in the Appeal Brief that the combination of Ko, Georgiou and McDermott does not disclose a performance demanding level input for determining the rate of reduction of the temperature-related frequency.

Now, the question before us is what Ko, Georgiou and McDermott would have taught to one of ordinary skill in the art? To answer this question, we find the following additional facts:

1. At column 6, lines 32 through 43, Ko states the following:

> **The clock arbiter 51 also changes from the max state to the hold state in response to an overheat signal latched from the temperature sensing circuit 49 during each cycle of clock 44.** This state change is shown by path 75 in FIG. 6 which indicates

> that the temperature is greater than an acceptable temperature T_{OK} (i.e., an overheat condition). During the next cycle of clock 44, the clock arbiter 51 again latches in the overheat signal from temperature sensing circuit 49. **If the overheat signal is still active, indicating that the overheat condition still exists, then clock arbiter 51 assumes the down state as shown by path 77 in FIG. 6, and activates the down output. [Emphasis added].**

Ko is concerned with managing the amount of power consumed in a single chip data processing device. Particularly, Ko teaches a temperature sensing circuit (49) that determines the temperature of a processor and forwards an overheat signal to a clock arbiter (51), which in turn activates a corresponding output signal of the clock arbiter that selects a lower clock frequency rate capable of reducing the amount of power dissipated in the processor. One of ordinary skill in art would have readily recognized that Ko's teaching of reducing the clock frequency in response to an indication of the processor being overheated amounts to the claimed limitation of a PDL input that determines a rate of reduction of the temperature-related frequency. In addition, as noted in the discussion of claim 1 above, such limitation is also taught by Georgiou. In consequence, we do not find error in the examiner's stated position, which concludes that the combination of Ko, Georgiou

and McDermott teaches the claimed limitation of a performance demanding level input for determining the rate of reduction of the temperature-related frequency. It is therefore our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would have suggested to the ordinarily skilled artisan the invention as set forth in claims 18 through 20. Accordingly, we will sustain the Examiner's obviousness rejection of claims 18 through 20.

CONCLUSION

In view of the foregoing discussion, we have sustained the Examiner's decision rejecting claims 1 through 20 under 35 U.S.C. § 103. Therefore, we affirm.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

JAMES D. THOMAS)
Administrative Patent Judge)
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) BOARD OF PATENT
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